**4013 D Type Flip Flop Page 38.1**

* On the rising edge of the clock pulse, the input D is copied to the output Q.
* This is called edge triggered. If the DATA input changes between clock pulses, this has no effect on the output.
* The rising edge of the clock pulse stores the input bit so this flip flop can be used as a data latch (memory).
* A single D Type Flip Flop can store one bit.
* On the rising edge of the clock pulse, if Q = 1 the circuit is "SET". If Q = 0 the circuit is "RESET".

**Here is the symbol of a D Type Flip Flop.**

|  |  |
| --- | --- |
| D Type Flip Flop.gif | 4013.gif |

* The device can be set or reset at any time by setting the S or R inputs high.
* This applies to AQA exam questions and 4000 series gates.

## Data Latch

Store bits of data on the rising edge of the clock pulse.

|  |  |
| --- | --- |
| D Type Flip Flop Latch.gif | * On the rising edge of the clock pulse, the data on D0, D1, D2 and D3 is copied to Q0, Q1, Q2 and Q3.
* Data latches are needed to store data that is only available or valid for a short time.
* For example data from the parallel port may not be valid for long.
* If this data is latched (stored), the latch output remains available for as long as necessary.
* The data remains valid until the next clock pulse.
 |

## Frequency Divider

**On the rising edge of the clock pulse, D is copied to Q.
Since NOT Q is connected to D, the data is inverted on each rising edge.
This has the effect of dividing the frequency by two.**

* The D Type Flip Flop is used in Binary Counters.
* Here is the circuit for a one bit counter.
* This can also be used as a frequency divider. It divides the frequency by two.
* The UP in Up Counter is because the counter counts normally with increasing numbers 0, 1, 2, 3 etc.
* The output of this circuit is high for 50% of the time and low for 50% of the time.
* This is a 1:1 mark space ratio.
* This is true whatever the mark space ratio of the clock pulses.



## Three Bit Binary Up Counter

This divides the frequency by 8 (or by two three times).



Here is a timing diagram for the three bit counter.



## Modulo N Up Counter

This is a counter that resets at a chosen number. For example a two digit decimal counter, left to its own devices will count from 00 to 99. This is not much use for a clock unless you have 100 second minutes. To fix the problem, the counter must go from 00 to 59. This is achieved by detecting a 6 in the left hand digit and using it to reset the counter to zero. This would be a Modulo 6 Counter or 60 if you included both digits.

## Modulo 6 Counter - Counts from 0 to 5



The circuit above detects a six or 0110 in binary. You could use the fool proof circuit but in fact the simpler circuit works too because the 0110 pattern only occurs once between 0 and 9 in decimal numbers. The output is used to reset the counter.

Here is a timing diagram for the modulo 6 counter. It shows the count going from 0 to 5 in regular time steps. The counter reaches 6 but only for about a microsecond before it resets to zero.



## Down Counter

This counter counts down towards zero.

The clock inputs come from the preceding Q instead of NOT Q .



## Shift Registers

* On the rising edge of the clock pulse, each D is copied to the next Q.
* The data moves one place to the right along the shift register like suitcases on a conveyor belt.
* Pulses can be delayed using this circuit.
* Shift registers can be used in simple combination locks.
* The registers have to be clocked in the correct sequence to unlock the door.



## Combinational and Sequential Logic

**Combinational Logic: Logic gates but there is No Clock and No Memory**

* The output is determined by combinations of one or more inputs.
* There is no clock signal.
* The circuits have no memory.
* The circuits are asynchronous (no clock).
* The output changes immediately when the input changes.

**Sequential Logic: Logic gates with a Clock and Memory**

* If your circuit has a clock, counters, or D-Type Flip-Flops, it is Sequential Logic.